LOW POWER DESIGN OF ELECTRICAL CIRCUITS PROJECT

Very low voltage operation of a 16-bit counter

Ziyan Xu

12/04/07

Introduction

- Course of project ——Reduction of voltage supply
- Aim —— Finding an optimum voltage
- Theory

  Dynamic Power

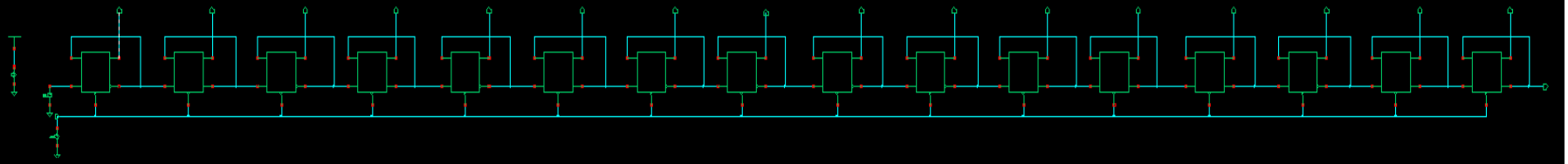
  $P = CV_{DD}^2 f$

  Delay

  $Delay = KV_{DD} / (V_{DD} - V_t)^{alpha}$

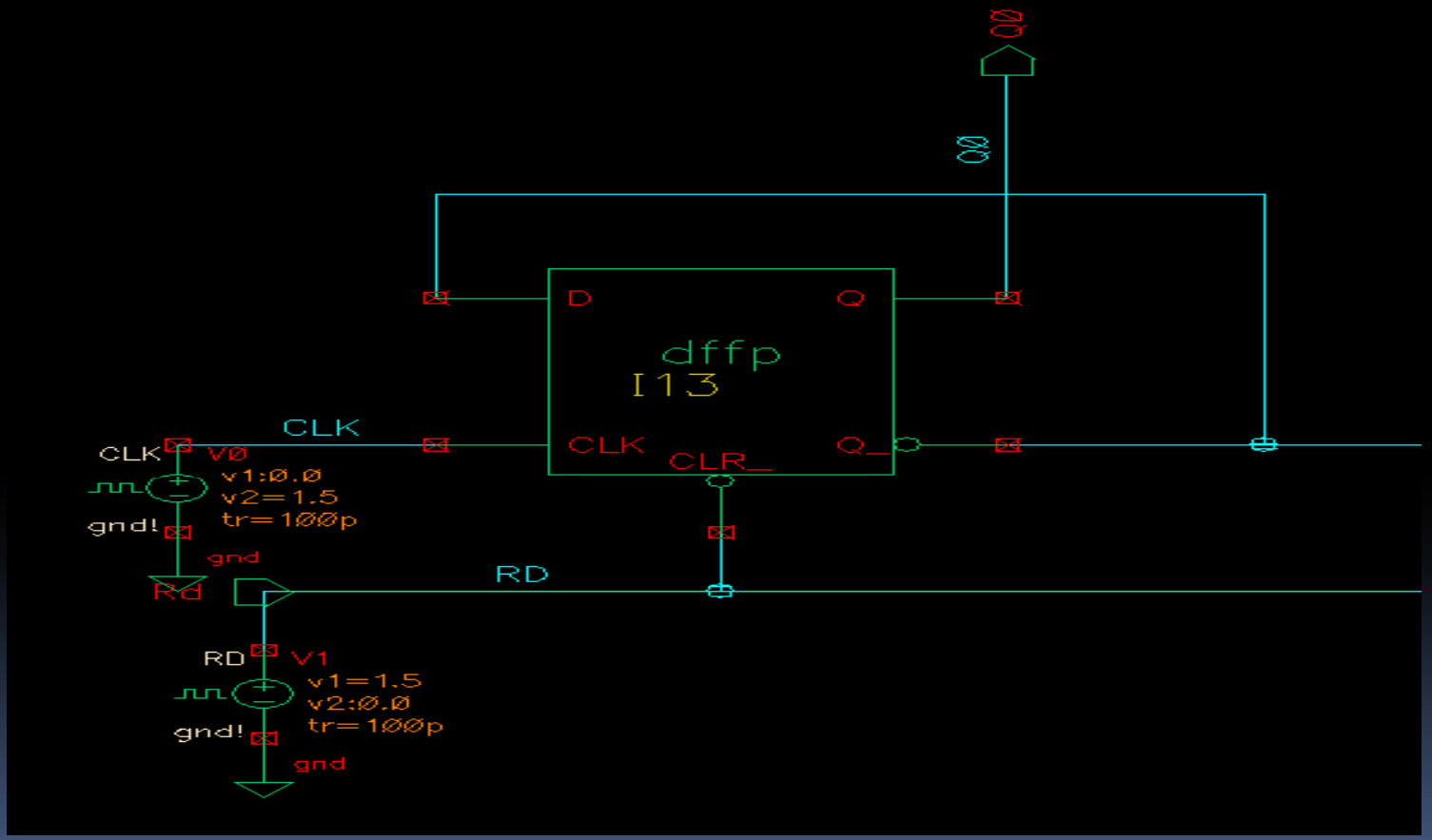
Circuit Design

- 16 bit counter



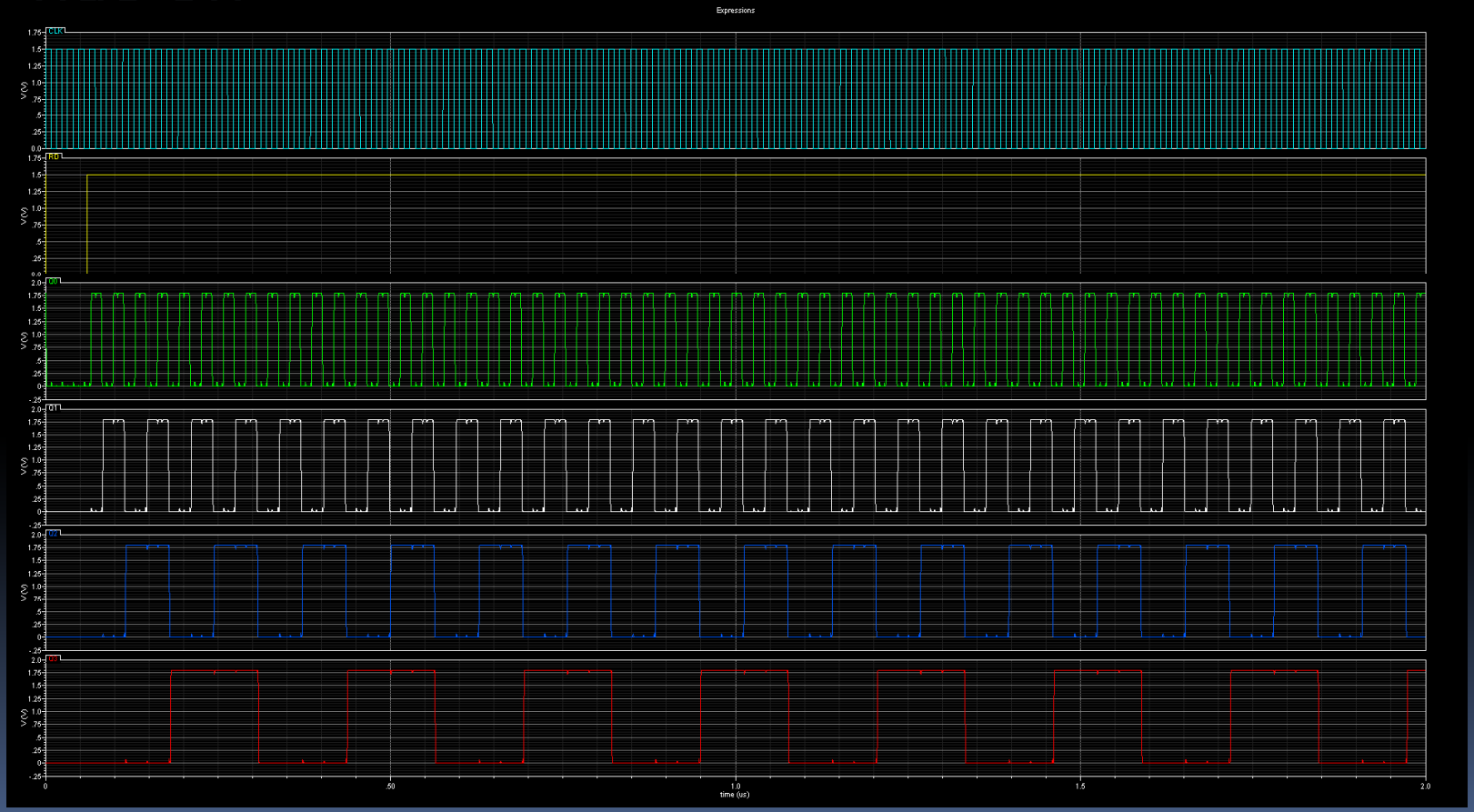
Circuit Design

- Rising Edge Triggered D Flip-Flop



Circuit Design

- Waveform



Simulation

- Device 0.5μm process
  Vth=0.6V
- Simulator
  Cadence Spectre
- Clock Frequency
  Clock Period=16ns
- Analysis Time
  T = 4μs

Simulation

- Results

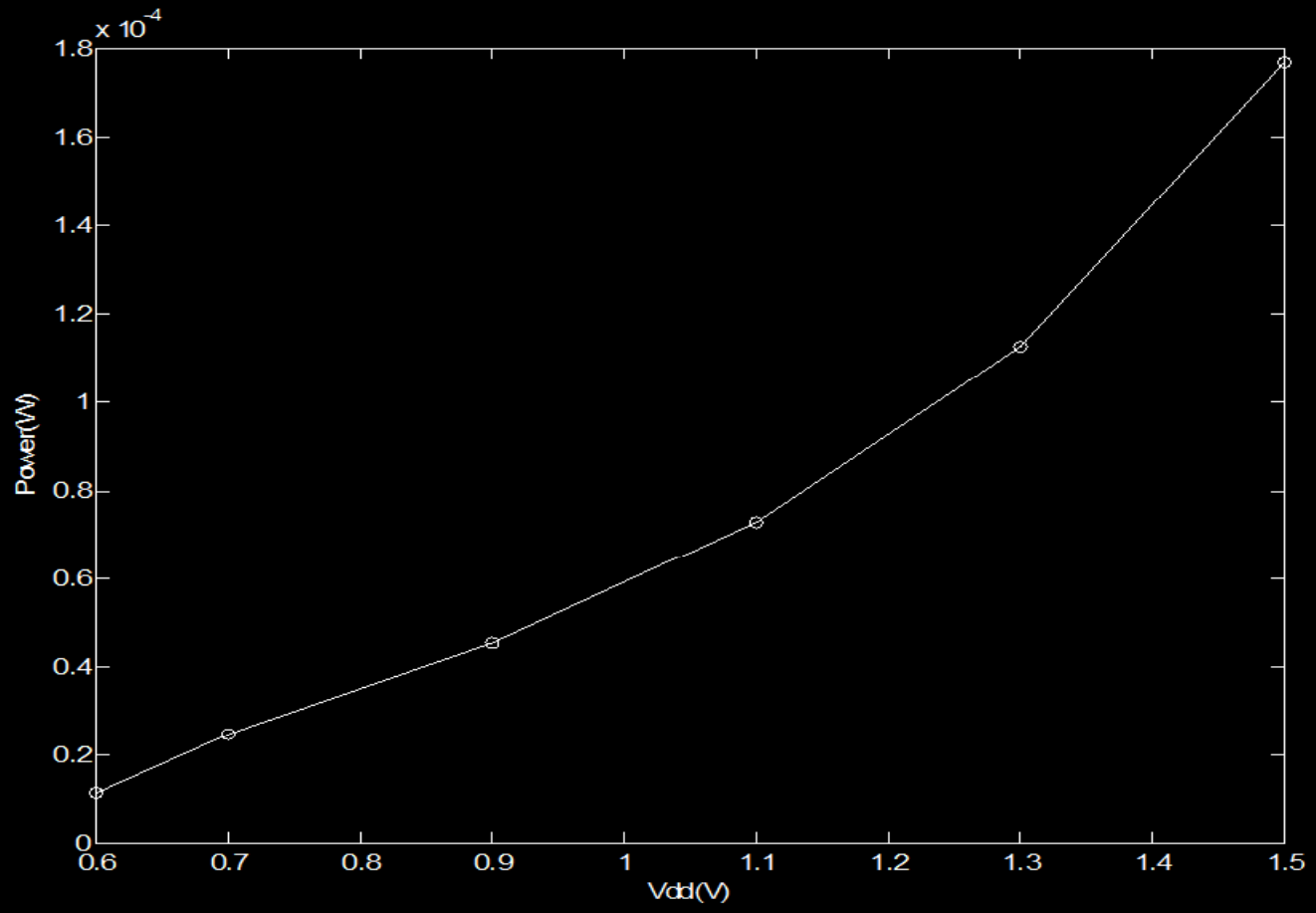
  Power=Vdd*∫ I dt/T

  Delay=16*$Delay_{clk\text{-}Q_0}$

Vdd(V)	Power(W)	Delay(s)	Power*Delay(W.S)
1.5	176.8E-6	5.24E-9	9.26E-13
1.3	112.5E-6	5.68E-9	6.39E-13
1.1	73.0E-6	7.49E-9	5.47E-13
0.9	45.1E-6	1.23E-8	5.55E-13
0.7	24.7E-6	3.20E-8	7.90E-13
0.6	11.2E-6	7.95E-8	8.9E-13
0.5	Fail to work		

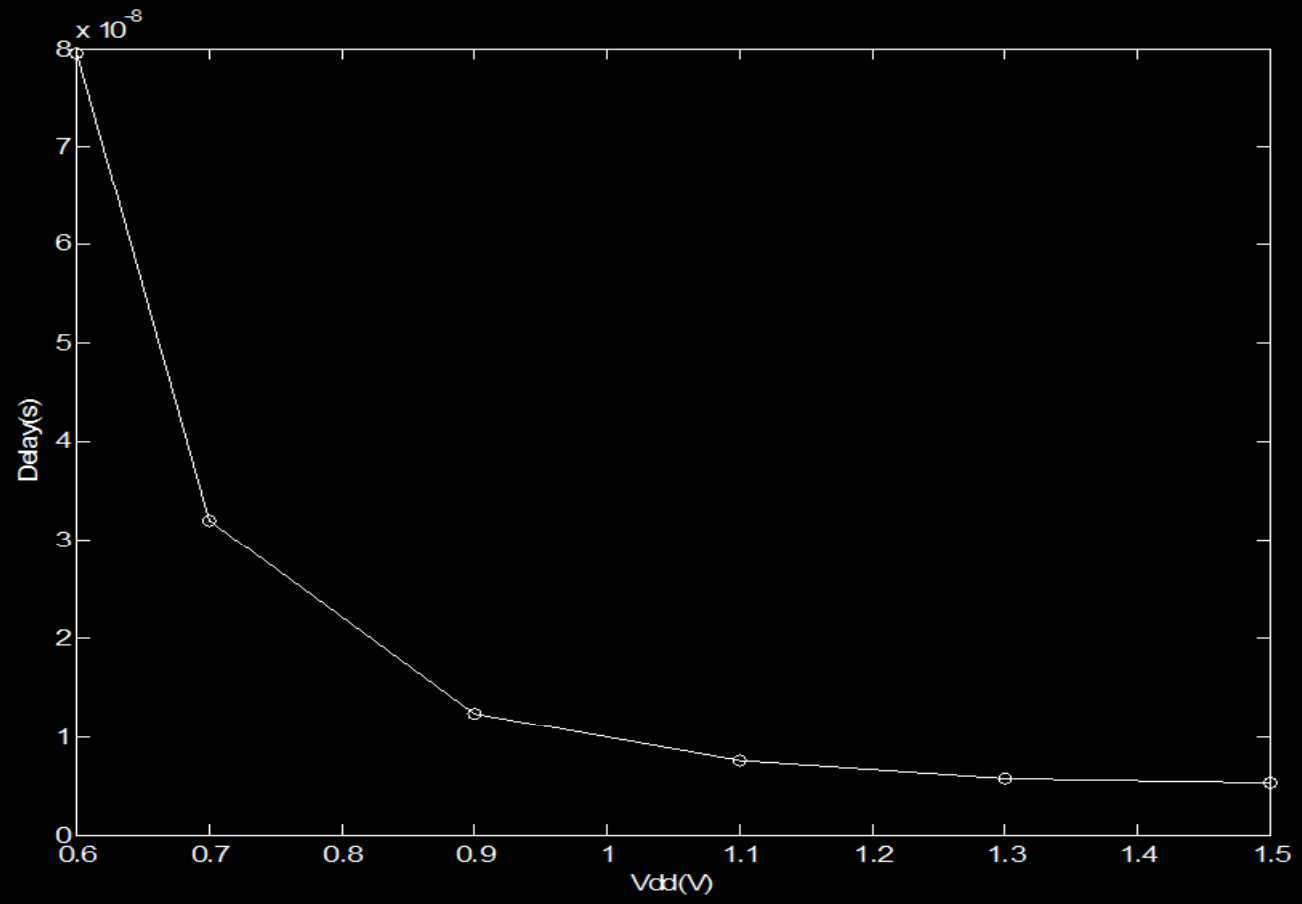
Simulation

- Power



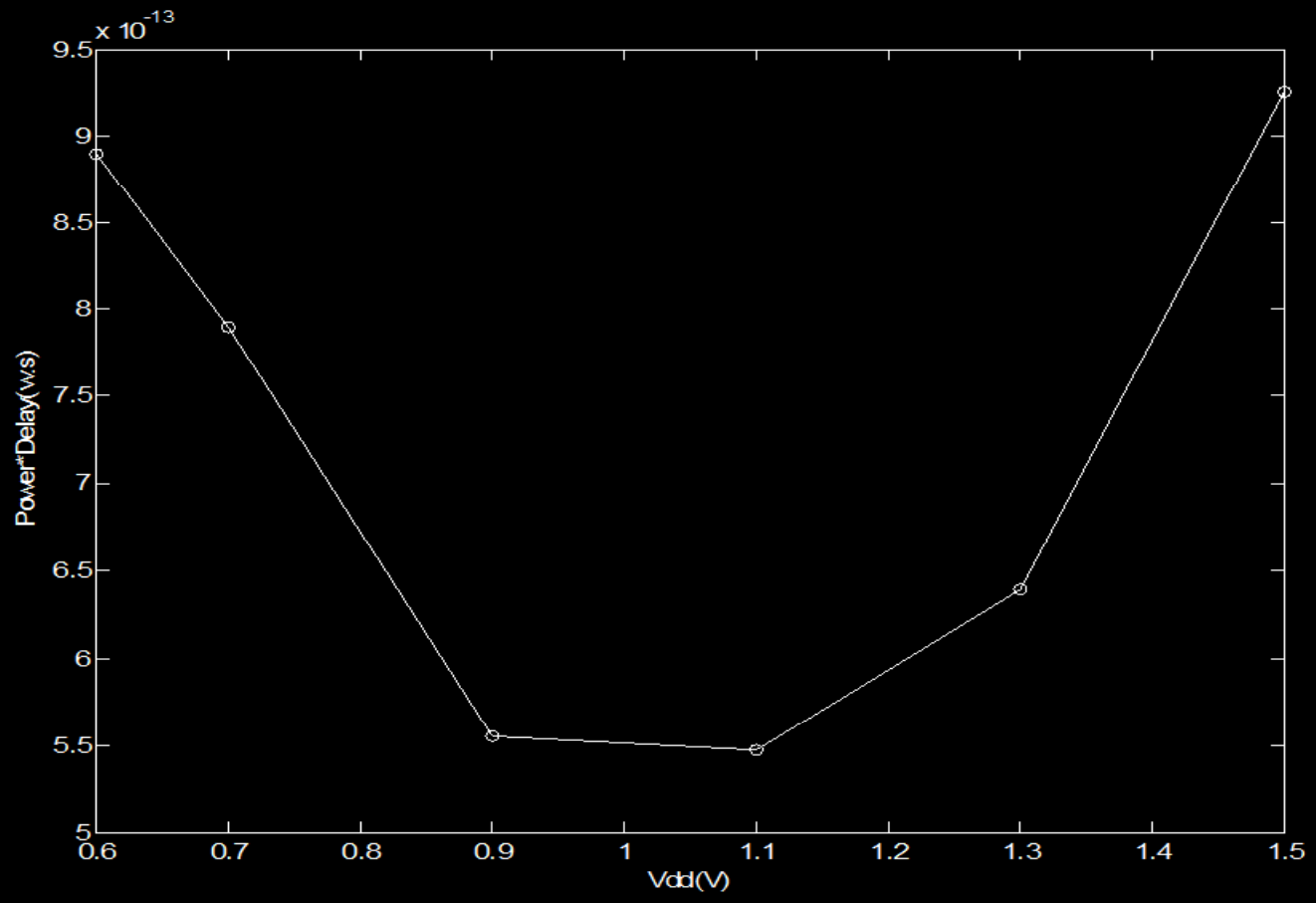
Simulation

- Delay



Simulation

- Power-Delay Product



Conclusion

- Substantial decrease in power by decreasing voltage.
- At lower voltages the increase in delay is greater than at higher voltages.
- The optimum supply voltage is between 0.9V~1.1V.

Extension

- Low –voltage limitation of MOSFETs

$$Vgs = Vt + \sqrt{\frac{I_d}{K}}\frac{L}{W}$$

Vt: Threshold Voltage

L and W: Effective dimensions of the gate length and width

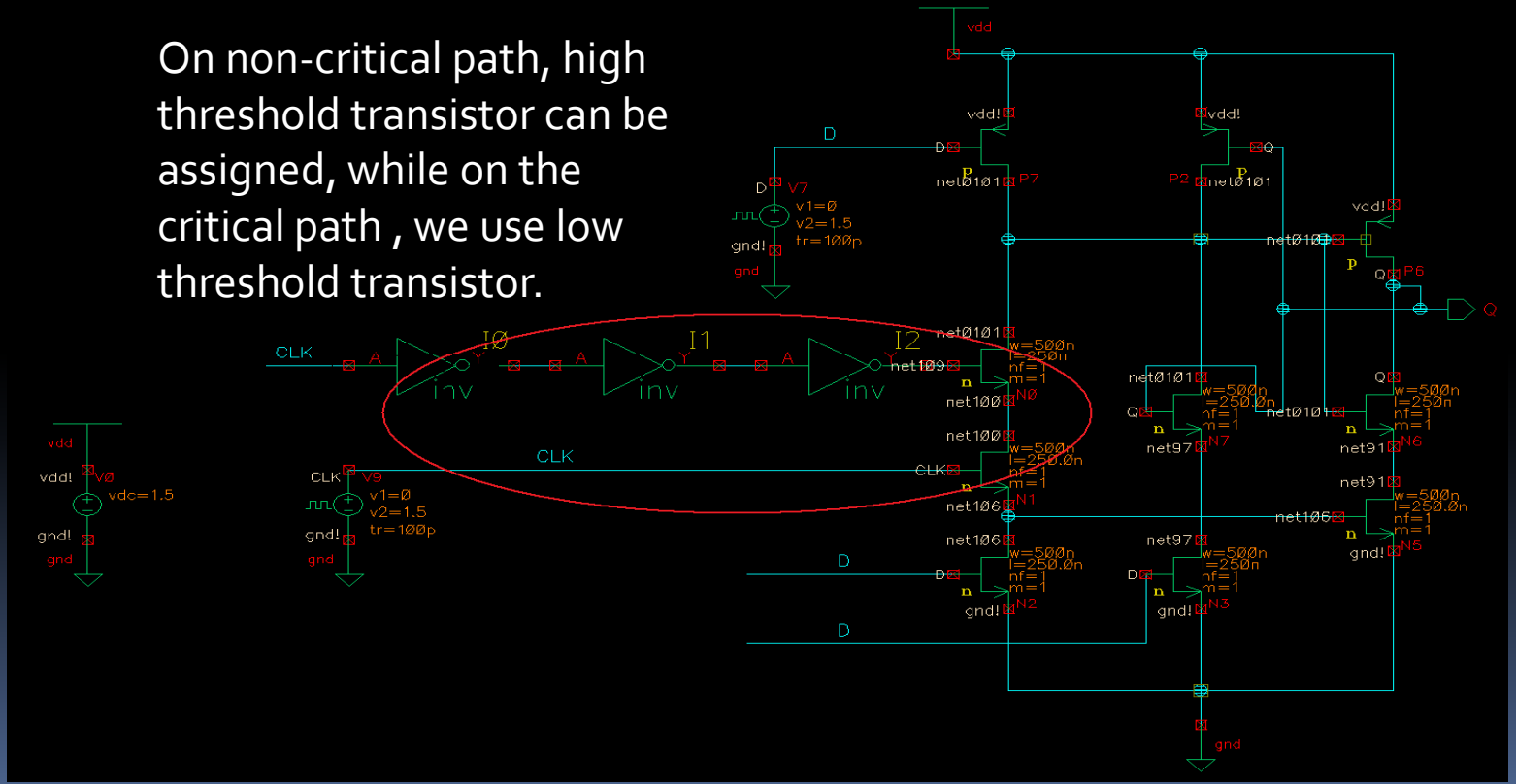
I_d : Drain current

K : Transconductance factor for the MOSFET

Extension

- Reduce leakage power——
  Multithreshold Technique

On non-critical path, high threshold transistor can be assigned, while on the critical path , we use low threshold transistor.



Reference

- Dr. V. Agrawal's ELEC 6970 slides, Lecture 5
- Wayn Wolf, Modern VLSI Design, Third Edition,Prentice-Hall, p.250-p.260
- B. Hoppe, Chr. Kroh, H.Meuth and M.Stohr ,A 440MHZ 16 Bit Counter in Cmos Standard Cells, ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International p.241-p.244
- H.Zhang, J.She n, X.Gu,Design of Low-power D Flip-flop Based on Multithreshold Technique, Journal of Zhejiang University(Science Edition),2005, 32(2), p.165-p.168
- E.Sinencio,A.Andreou,Low-Voltage/Low-Power Integrated Circuits and Systems,Wiley-Interscience, 1998,p.68-p.70

Thanks!